REMARKS

Claims 1-16 are presented for examination. Claims 1 and 11 have been amended to more clearly define the invention.

The specification on page 10 has been amended to correct a typo. The element 12 in FIG. 5 is identified as "an interface portion," instead of "an interface." No new matter is added because a similar element 2 in FIG. 1 is identified on page 6 as "an interface portion."

FIG. 26 has been corrected to designate the horizontal axis in a waveform diagram as "TIME." No new matter is added because the waveform diagrams in FIGS. 24 and 29 also have the horizontal axes designated as "TIME."

Further, the Examiner asserts that the IDS filed on April 3, 2001 does not contain a list of all patents and publications. Therefore, the information contained in this IDS was not considered. It is noted that the PTO-1449 form contains a single publication which was filed with the IDS of April 3, 2001.

On October 1, 2003, the undersigned applicants' representative conducted a telephone conference with the Examiner to discuss this issue. The Examiner advised the applicants' representative that she did not receive this form, and requested that the form be submitted with a response to the Office Action.

Per Examiner's request, the PTO-1449 form is resubmitted, together with a mailing card confirming that this form was originally submitted on April 3, 2001.

Claims 1-13 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Motomura.

Independent claim 1, as amended, recites a semiconductor memory device, comprising:

- a terminal group receiving an externally applied control signal, address, and data;

- a memory cell array transmitting/receiving said data to/from a region designated by said address in accordance with said control signal; and

- a logic circuit processing data in accordance with at least one of said control signal, address, and data when said address designates a prescribed first region of the memory cell array if said control signal, address, and data are applied to said terminal group in a sequence of applying said control signal, address, and data to said memory cell array.

The Examiner considers:

- terminal 5 (FIG. 8 of Motomura) to correspond to the claimed terminal group;

- DRAM 15 to correspond to the claimed memory cell array; and

- control section 12 to correspond to the claimed logic circuit.

The Examiner relies upon col. 31, lines 2-12 and 28-35 for disclosing that the control section 12 processes data in accordance with at least one of the control signal, address, and data if the control signal, address, and data are applied to the terminal group in a sequence of applying the control signal, address, and data to the memory cell array.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989).

Considering the reference, Motomura discloses that the read data to be transmitted via the read data terminal and write data received via the write data terminal are transferred between the control section 12 and the DRAM 15 or memory control register 16 via the internal memory bus (col. 31, lines 2-12 and 28-35).

However, the reference does not disclose that the control section 12 processes data in accordance with at least one of the control signal, address, and data applied to the terminal 5, when the address designates a prescribed first region of the memory cell array, if the control signal, address, and data are applied to this terminal in a sequence of applying the control signal, address, and data to the memory cell array. Instead, Motomura teaches that memory sections 11 or coprocessor sections 14 in DRAMs 1 are uniquely designated by the device ID field (FIGS. 13A-13D, column 26, lines 1-6, 20-26).

Accordingly, Motomura does not disclose the logic circuit operating in the manner required by claim 1.

Independent claim 11 recites a method of controlling a semiconductor memory device including a terminal group receiving an externally applied control signal, address, and data, a memory cell array transmitting/receiving said data in accordance with said control signal to/from a region designated by said address, and a logic circuit processing data in accordance with at least one of said control signal, said address, and said data when said address designates a prescribed first region of the memory cell array if said control signal, said address, and said data are applied to said terminal group in a sequence of applying said control signal, said address and said data to said memory cell array. The method comprises:

- the step of designating said first region as a reserved region; and

- the step of designating said first region by said address in a sequence of writing to said memory cell array and applying a command to said logic circuit.

As discussed above, the reference does not disclose processing data in accordance with at least one of the control signal, address, and data, when the address designates a prescribed first region of the memory cell array, if the control signal, address, and data are applied to the

terminal group in a sequence of applying the control signal, address, and data to the memory cell array.

Further, Motomura does not disclose designating a reserved region by an address in a sequence of writing to the memory cell array and applying a command to the logic circuit.

The Examiner relies upon col. 30 and 31 of Motomura. However, she did not indicate specifically wherein the reference discloses designating the memory control register 29 (considered by the Examiner to correspond to the claimed first region) by an address in a sequence of writing to the DRAM 15 and applying a command to the control section 12. As demonstrated above, any memory section 11 of the DRAM is designated by a device ID field.

Hence, Motomura does not describe the method recited in claim 11.

Claims 2-10, 12 and 13 depend from the respective claims 1 or 11 and are defined over the reference at least for the reasons presented above in connection with claims 1 and 11.

Applicants, therefore, respectfully submit that the rejection of claims 1-13 under 35 U.S.C. § 102 as anticipated by Motomura is untenable and should be withdrawn.

Claims 14-16 have been rejected under 35 U.S.C. § 103 as being unpatentable over Motomura in view of Maruyama et al.

It is noted that the Maruyama et al. patent is available only as a reference under 35 U.S.C. § 102(e). The applicants submit that subject matter of this patent and the claimed invention were, at the time the invention was made, owned by the same company or subject to an obligation of assignment to the same company.

Therefore, the Maruyama patent is not available as a reference under 35 U.S.C. § 103.

Accordingly, the rejection of claims 14-16 under 35 U.S.C. § 103 as being unpatentable over Motomura in view of Maruyama et al. should be withdrawn.

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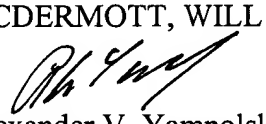
In view of the foregoing, and in summary, claims 1-16 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Alexander V. Yampolsky
Registration No. 36,324

Attachments: Replacement Sheet FIG. 26
PTO Form 1449 dated Apr. 3, 2001
Mailing and Return Courier Cards dated Apr. 3, 2001

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 AVY:MWE
Facsimile: (202) 756-8087
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